Simon Deleonibus

MSc and PhD in Applied Physics from Paris University, in 1979 and 1982 respectively.

Since 2008, he is Chief Scientist (Directeur Scientifique) at LETI watching at the Silicon Technologies Research (850 researchers).

From 1999 to 2008, he was Director of the Electronic Nanodevices Laboratory(60 researchers). He managed several Industrial, National and European funded projects.

From 1996 to 1999, he managed the Ultimate CMOS project.

He joined LETI(CEA) in 1986 as a device engineering and process modules development expert for CMOS and Flash memories applications.

He joined Thomson Semiconducteurs (Grenoble) in 1981 as a development and transfer to production process integration engineer.

Published papers or submitted: more than 550 (conferences and journals ; 60 invited) .

Editor of 1 book (WSPC). Guest editor of 1 Special issue of SSE. Author of 7 book chapters.

Editor of IEEE Transactions on Electron Devices.

Editor for European Physical Journal - EPJ Applied Physics

He owns 30 patents: among them the initial patent on contact plug principle, widely used as a standard process by the semiconductor industry.

With his team, he realized the first 20nm gate length MOSFET, world's smallest transistor in June 1999.

International Conference program Committees. European Chair and Member of the VLSI Technology Symposium(from 2000 to 2006). Member of the 1998 and 1999,2004 and 2005 International Electron Devices Meeting (IEDM) program committtee. Member of the ESSDERC program committee since 2000 and Responsible for the ESSDERC2005 Tutorials. Member of the International Technology Roadmap of Semiconductors(ITRS). Member of the Board of Directors of the Nanosciences Foundation. Member of the European Research Council Engineering Panel.

Since 1998, he lectures on microelectronics devices physics and technology and nanosciences in different Institutions and Universities, in France and Worldwide.

Fellow of the IEEE .
Research Director of French CEA.
IEEE Distinguished Lecturer.
"Chevalier de l'Ordre National du Mérite" Decree of French Presidence .
Recipient of the "2005 Grand Prix de l'Académie des Technologies - Prix Chéreau Lavet".
Recipient or co-recipient of 10 Best Papers Awards obtained in International conferences.

Member of the Electrochemical Society; Member of the Materials Research Society.

Recent selected publications authored by Simon Deleonibus

Invention of contacts plugs in 1984

[1] **S.Deleonibus** and G.Dubois for THOMSON-SEMICONDUCTORS, "Planarized contacts for integrated circuits. Plugs obtained by conformal deposition and etch-back" Patent April 1984 France National registration n°: 84.05906. Extended to U.S.A. in April 1985 (file N° 721,779) (1st inventor)

[2] A.Bergemont, **S.Deleonibus**, B.Guillaumot, M.Laurens, F.Martin, G.Guegan " A high performance CMOS process for submicron 16Mbit EPROM", Proceedings of IEDM'89, pp.591, Washington(D.C.), Dec. 1989 (Technical leader module development)

World's record of smallest transistor in 1999

[3] **S.Deleonibus**, C.Caillat, G.Guegan, M. Heitzmann, M.-E. Nier, S.Tedesco, B.Dal Zotto, F.Martin, P.Mur, A.-M.Papon, G.Lecarval, S. Biswas "A 20 nm physical gate length NMOSFET featuring 1.2 nm gate oxide shallow implanted source and drains and BF2 pockets." Electron Devices Letters, pp. 173-175, April 2000.(Projet leader)

[4] **S.Deleonibus** "Alternative CMOS or alternative to CMOS ?" (**Invited paper**) Microelectronics Reliability, vol 41/1,pp. 3-12,Elsevier Publisher, Jan. 2001(Projet leader)

[5] X. Jehl, M. Sanquer, G. Bertrand. G. Guégan, **S. Deleonibus**, and D. Fraboulet, (**Invited talk and paper**) "MOSFET and/or MOS SET: which way to go for silicon nanoelectronics?", Silicon Nanoelectronics Workshop, Kyoto, 6-2003, published in IEEE Transactions on Nanoelectronics, vol. 2, N° 4, pp 308-313, Dec. 2003 (Laboratory Director)

Development of technology modules for Si CMOS Micro and Nanoelectronics

[6] **S.Deleonibus** " Field isolation for the Gigabit era devices" (**Invited paper and talk**) Proceedings ESSDERC'93, pp391-398, Grenoble, Sept.11-16 1993 (Technical leader module development)

[7]**S.Deleonibus** "Is there LOCOS after LOCOS ?" (**Invited paper and talk**) Proceedings 7th ESPRIT Workshop on Dielectrics for Microelectronics Heraklion-Crete(Greece), 22-24 Nov. 1995 *Published in Solid State Electronics, Elsevier Publishers1997.* (Technical leader module development)

[8]T. Ernst, J.M. Hartmann, V. Loup, F. Ducroquet, P. Dollfus, G. Guegan, D. Lafond, P. Holliger, B. Prévitali, A. Toffoli, and **S. Deleonibus**, "Fabrication of a novel strained SiGe:C-channel planar 55nm nMOSFET for High-Performance CMOS" Proceedings of VLSI Technology Symposium, p. 92-93, June 2002, Honolulu (USA) (Laboratory Director)

[9] T. Ernst, F. Ducroquet, J.M. Hartmann, O. Weber, V. Loup, R. Truche, A.M. Papon, P. Holliger, L. Brévard, A. Toffoli, J.L. Di Maria and **S. Deleonibus**, "A new Si:C epitaxial channel nMOSFET with architecture with improved drivability and short channel characteristics, Proceedings of VLSI Technology Symposium, pp51-52, June 2003., Kyoto (Japan). (Laboratory Director)

[10]B Guillaumot, X Garros, F Lime, K Oshima, B Tavel, J.A. Chroboczek, P Masson, R Truche, A M Papon, F Martin, JF Damlencourt, S Maitrejean, M Rivoire, C Leroux, S Cristoloveanu, G Ghibaudo JL Autran, T Skotnicki **, S.Deleonibus** " 75nm Damascene Metal Gate and High-k Integration for Advanced CMOS Devices" Tech Digest IEDM 2002 p 355-358, San Francisco(CA), Dec 2002 (Laboratory Director)

[11] M. Vinet, T. Poiroux, J. Widiez , J. Lolivier, B. Previtali, C. Vizioz, B. Guillaumot, P. Besson, J. Simon, F. Martin, S. Maitrejean, P. Holliger, B. Biasse, M. Cassé, F. Allain, A. Toffoli, D. Lafond, J.M. Hartmann, R. Truche, V. Carron, F. Laugier, A. Roman ,Y. Morand , D. Renaud, M. Mouis and **S. Deleonibus,** "Planar Double Gate CMOS transistors with 40nm metal gate for multipurpose applications" Proceedings SSDM2004, pp768-769 , Tokyo(Japan) Sept 2004, **Best paper Award** (Laboratory Director)

[12] J. Widiez, F. Daugé, M. Vinet, T. Poiroux, B. Previtali, M. Mouis and **S. Deleonibus**, "Experimental Gate Misalignment Analysis on Double Gate SOI MOSFETs",Proceedings IEEE International SOI Conference 2004, pp 185-186,Charleston(SC), October 2004 ,**Best paper Award** (Laboratory Director)

[13] B. De Salvo , C. Gerardi , S. Lombardo , T. Baron , L. Perniola , D. Mariolle , P. Mur , A. Toffoli , M. Gely , M .N. Semeria , **S. Deleonibus**, G. Ammendola , V. Ancarani, M. Melanotte, R. Bez , L. Baldi, D. Corso, I. Crupi , R. A. Puglisi , G. Nicotra, E. Rimini, F. Mazen, G. Ghibaudo, G. Pananakakis ,C. Monzio Compagnoni , D. Ielmini , A. Lacaita, A. Spinelli , Y. M. Wan, K .van der Jeugd "How far will Silicon nanocrystals push the scaling limits of NVMs technologies?", Technical Digest of IEDM 2003, Washington D.C., December 2003. (Laboratory Director)

[14] **S.Deleonibus** "Devices Architectures for the nano CMOS era" Chapter 5.2 in *Fundamental and Technological Aspects of High-K gate Dielectrics*, Institute of Physics Publisher, pp. 524-559, London 2003. (Laboratory Director and Projectr leader)

[15] **S. Deleonibus,** B. de Salvo, T. Ernst, O.Faynot, T. Poiroux, P.Scheiblin, M. Vinet, "CMOS Devices Architectures and Technology Innovations for the Nanoelectronic Era " (**Invited talk and paper**)**,** Proceedings of WOFE-2004 **,** Aruba 17-23 December 2004, published in International Journal of High Speed Electronics and Systems, vol. 16, No.1(2006), pp. 193-219. (Laboratory Director and Projectr leader)